

Pre-settable synchronous 4-bit binary counter; asynchronous reset

74LVC161

FEATURES

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. JESD8B/JESD36
- Asynchronous reset
- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- ESD protection:
 - HBM EIA/JESD22-A114-B exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

DESCRIPTION

The 74LVC161 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC161 is a synchronous pre-settable binary counter which features an internal look-head carry and can be used for high-speed counting. Synchronous operation

is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (pin CP). The outputs (pins Q0 to Q3) of the counters may be preset to a HIGH-level or a LOW-level. A LOW-level at the parallel enable input (pin $\overline{\text{PE}}$) disables the counting action and causes the data at the data inputs (pins D0 to D3) to be loaded into the counter on the positive-going edge of the clock (provided that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (pins CEP and CET). A LOW-level at the master reset input (pin $\overline{\text{MR}}$) sets all four outputs of the flip-flops (pins Q0 to Q3) to LOW-level regardless of the levels at input pins CP, $\overline{\text{PE}}$, CET and CEP (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (pins CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (pin TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH-level output of Q0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by t_{PHL} (propagation delay CP to TC) and t_{su} (set-up time CEP to CP) according to the following

$$\text{formula: } f_{\text{max}} = \frac{1}{t_{\text{PHL}(\text{max})} + t_{\text{su}}}$$

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QUICK REFERENCE DATAGND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f \leq 2.5\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Qn CP to TC \overline{MR} to Qn \overline{MR} to TC CET to TC	$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	3.9 4.5 3.5 4.7 3.3	ns ns ns ns ns
$f_{clk(max)}$	maximum clock frequency		200	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	18	pF

Notes

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$$
 where:

 f_i = input frequency in MHz;

 f_o = output frequency in MHz;

 C_L = output load capacitance in pF;

 V_{CC} = supply voltage in Volts;

 N = total load switching outputs;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

- The condition is $V_I = \text{GND}$ to V_{CC} .

ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC161D	-40 °C to +125 °C	16	SO16	plastic	SOT109-1
74LVC161DB	-40 °C to +125 °C	16	SSOP16	plastic	SOT338-1
74LVC161PW	-40 °C to +125 °C	16	TSSOP16	plastic	SOT403-1
74LVC161BQ	-40 °C to +125 °C	16	DHVQFN16	plastic	SOT763-1

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low voltage applications	1.2	3.6	V
V _I	input voltage		0	5.5	V
V _O	output voltage		0	V _{CC}	V
T _{amb}	operating temperature	in free-air	-40	+125	°C
t _r , t _f	input rise and fall times	V _{CC} = 1.2 V to 2.7 V	0	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{CC}	supply voltage		-0.5	-	+6.5	V
I _{IK}	input diode current	V _I < 0 V	-	-50	-	mA
V _I	input voltage	note 2	-0.5	-	+6.5	V
I _{OK}	output diode current	V _O > V _{CC} or V _O < 0 V	-	±50	-	mA
V _O	output voltage	note 2	-0.5	-	V _{CC} + 0.5	V
I _O	output source or sink current	V _O = 0 V to V _{CC}	-	±50	-	mA
I _{CC} , I _{GND}	V _{CC} or GND current		-	±100	-	mA
T _{stg}	storage temperature		-65	-	+150	°C
P _{tot}	power dissipation	T _{amb} = -40 °C to +125 °C; note 3	-	500	-	mW

Notes

- Stresses beyond those listed may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other condition beyond those indicated under "Recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO16 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP16 and TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

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DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 °C to +85 °C							
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	-	-	V
			2.7 to 3.6	2.0	-	-	V
V _{IL}	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 μA	2.7 to 3.6	V _{CC} - 0.2	V _{CC}	-	V
		I _O = -12 mA	2.7	V _{CC} - 0.5	-	-	V
		I _O = -18 mA	3.0	V _{CC} - 0.6	-	-	V
		I _O = -24 mA	3.0	V _{CC} - 0.8	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μA	2.7 to 3.6	-	GND	0.2	V
		I _O = 12 mA	2.7	-	-	0.4	V
		I _O = 24 mA	3.0	-	-	0.55	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.6	-	±0.1	±5	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A	3.6	-	0.1	10	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} - 0.6 V; I _O = 0 A	2.7 to 3.6	-	5	500	μA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 °C to +125 °C							
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	-	-	V
			2.7 to 3.6	2.0	-	-	V
V _{IL}	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 μA	2.7 to 3.6	V _{CC} - 0.3	-	-	V
		I _O = -12 mA	2.7	V _{CC} - 0.65	-	-	V
		I _O = -18 mA	3.0	V _{CC} - 0.75	-	-	V
		I _O = -24 mA	3.0	V _{CC} - 1	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μA	2.7 to 3.6	-	-	0.3	V
		I _O = 12 mA	2.7	-	-	0.6	V
		I _O = 24 mA	3.0	-	-	0.8	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.6	-	-	±20	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A	3.6	-	-	40	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} - 0.6 V; I _O = 0 A	2.7 to 3.6	-	-	5000	μA

Note

1. Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

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AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500$ Ω .

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 °C to +85 °C; note 1							
t _{PHL} /t _{PLH}	propagation delay CP to Qn	see Figs 9 and 14	1.2	–	17	–	ns
			2.7	1.5	–	7.2	ns
			3.0 to 3.6	1.5	3.9 ⁽²⁾	7.3	ns
	propagation delay CP to TC	see Figs 9 and 14	1.2	–	20	–	ns
			2.7	1.5	–	7.8	ns
			3.0 to 3.6	1.5	4.5 ⁽²⁾	7.8	ns
	propagation delay CET to TC	see Figs 10 and 14	1.2	–	16	–	ns
			2.7	1.5	–	6.5	ns
			3.0 to 3.6	1.5	3.3 ⁽²⁾	6.0	ns
t _{PHL}	propagation delay \overline{MR} to Qn	see Figs 11 and 14	1.2	–	17	–	ns
			2.7	1.5	–	7.1	ns
			3.0 to 3.6	1.5	3.5 ⁽²⁾	6.4	ns
	propagation delay \overline{MR} to TC	see Figs 11 and 14	1.2	–	18	–	ns
			2.7	1.5	–	8.6	ns
			3.0 to 3.6	1.5	4.7 ⁽²⁾	8.0	ns
t _w	clock pulse width HIGH or LOW	see Fig.9	2.7	5.0	–	–	ns
			3.0 to 3.6	4.0	1.2 ⁽²⁾	–	ns
	master reset width LOW	see Fig.11	2.7	4.0	–	–	ns
			3.0 to 3.6	3.0	1.6 ⁽²⁾	–	ns
t _{rem}	removal time \overline{MR} to CP	see Fig.11	2.7	0.0	–	–	ns
			3.0 to 3.6	0.5	0.0 ⁽²⁾	–	ns
t _{su}	set-up time Dn to CP	see Fig.12	2.7	3.0	–	–	ns
			3.0 to 3.6	2.5	1.0 ⁽²⁾	–	ns
	set-up time \overline{PE} to CP	see Fig.12	2.7	3.5	–	–	ns
			3.0 to 3.6	3.0	1.2 ⁽²⁾	–	ns
	set-up time CEP, CET to CP	see Fig.13	2.7	5.5	–	–	ns
			3.0 to 3.6	5.0	2.1 ⁽²⁾	–	ns
t _h	hold time Dn, \overline{PE} , CEP, CET to CP	see Figs 12 and 13	2.7	0.0	–	–	ns
			3.0 to 3.6	0.5	0.0 ⁽²⁾	–	ns
f _{clk(max)}	maximum clock frequency	see Fig.9	2.7	150	–	–	MHz
			3.0 to 3.6	150	200 ⁽²⁾	–	MHz
t _{sk(0)}	skew	note 3	3.0 to 3.6	–	–	1.0	ns

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SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 °C to +125 °C							
t _{PHL} /t _{PLH}	propagation delay CP to Qn	see Figs 9 and 14	1.2	–	–	–	ns
			2.7	1.5	–	9.0	ns
			3.0 to 3.6	1.5	–	9.5	ns
	propagation delay CP to TC	see Figs 9 and 14	1.2	–	–	–	ns
			2.7	1.5	–	10.0	ns
			3.0 to 3.6	1.5	–	10.0	ns
	propagation delay CET to TC	see Figs 10 and 14	1.2	–	–	–	ns
			2.7	1.5	–	8.5	ns
			3.0 to 3.6	1.5	–	7.5	ns
t _{PHL}	propagation delay \overline{MR} to Qn	see Figs 11 and 14	1.2	–	–	–	ns
			2.7	1.5	–	9.0	ns
			3.0 to 3.6	1.5	–	8.0	ns
	propagation delay \overline{MR} to TC	see Figs 11 and 14	1.2	–	–	–	ns
			2.7	1.5	–	11.0	ns
			3.0 to 3.6	1.5	–	10.0	ns
t _w	clock pulse width HIGH or LOW	see Fig.9	2.7	5.0	–	–	ns
			3.0 to 3.6	4.0	–	–	ns
	master reset width LOW	see Fig.11	2.7	4.0	–	–	ns
			3.0 to 3.6	3.0	–	–	ns
t _{rem}	removal time \overline{MR} to CP	see Fig.11	2.7	0.0	–	–	ns
			3.0 to 3.6	0.5	–	–	ns
t _{su}	set-up time Dn to CP	see Fig.12	2.7	3.0	–	–	ns
			3.0 to 3.6	2.5	–	–	ns
	set-up time \overline{PE} to CP	see Fig.12	2.7	3.5	–	–	ns
			3.0 to 3.6	3.0	–	–	ns
	set-up time CEP, CET to CP	see Fig.13	2.7	5.5	–	–	ns
			3.0 to 3.6	5.0	–	–	ns
t _h	hold time Dn, \overline{PE} , CEP, CET to CP	see Figs 12 and 13	2.7	0.0	–	–	ns
			3.0 to 3.6	0.5	–	–	ns
f _{clk(max)}	maximum clock frequency	see Fig.9	2.7	150	–	–	MHz
			3.0 to 3.6	150	–	–	MHz
t _{sk(0)}	skew	note 3	3.0 to 3.6	–	–	1.5	ns

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. Typical values are measured at V_{CC} = 3.3 V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

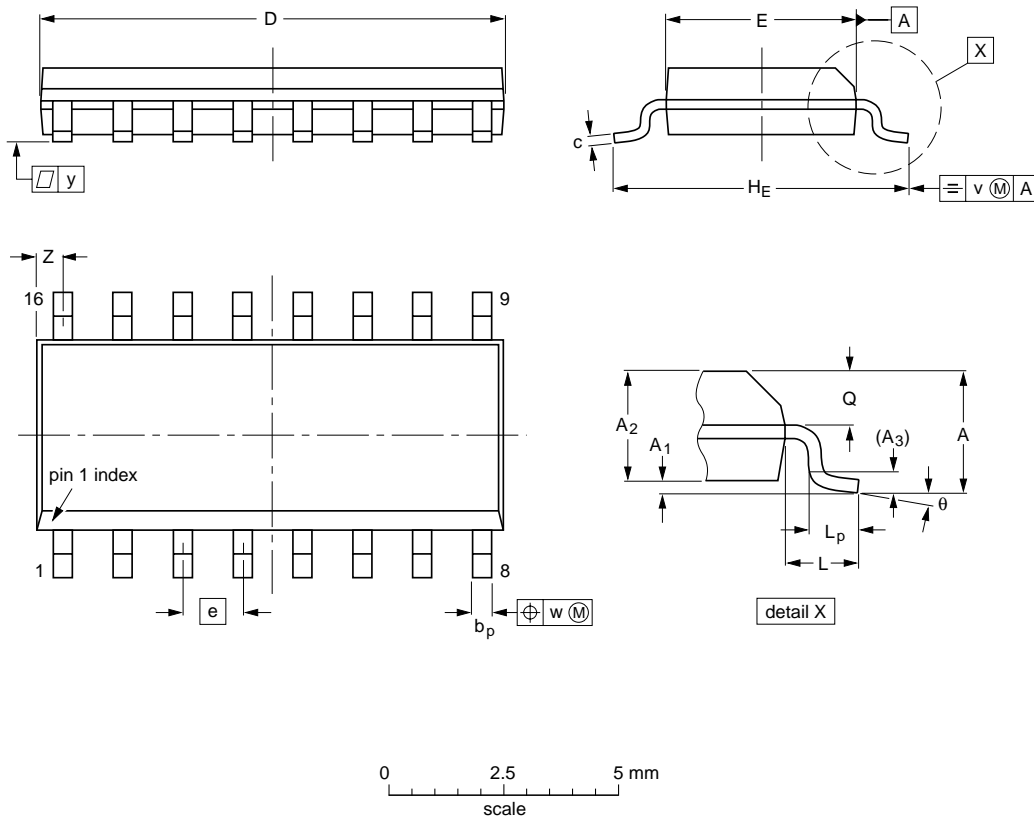
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PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION
	IEC	JEDEC	JEITA	
SOT109-1	076E07	MS-012		